DESIGN OF A DIGITAL MULTI-CHANNEL ANALYZER BASED ON FPGA FOR HPGe DETECTOR

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Abstract: This study presents a design of digital multi-channel analyzer (DMCA) based on Field-programmable gate array (FPGA) for HPGe detector. The main hardware of DMCA is implemented by using a 16-bit ADC with 105 Msps and Artix-7 FPGA. The algorithms of pulse shaping filter, detecting peaks and spectrum histogram processing are designed and simulated by using MATLAB. Therefore, the FPGA resources are optimized, leading to cost-effective hardware. Due to all algorithms implemented on FPGA, the DMCA performs in real-time. The pileup problem and baseline restoration are carefully processed to improve the energy resolution. The DMCA was examined with an HPGe detector of GC1518 model of Canberra with ^{137}Cs, ^{60}Co and ^{133}Ba sources. The energy resolution of the DMCA at 1332 keV ^{60}Co has attained 3.1 keV. With this result, the prototype system of the DMCA is highly promising for a multi-DMCA system in considering performance, cost and size.

Keywords: DMCA, FPGA, HPGe

I. INTRODUCTION

The pulse spectroscopy systems are widely applied in many areas such as in nuclear physics research, in industrial and medical applications. Due to their important roles, they have been developed since the early 1950s [1]. Pulse processing is a main objective in the pulse spectroscopy to minimize distortion and electronic noise, and to increase performance and accuracy. A system for traditional analogical signal processing, which consists of a preamplifier, amplifier, analog pulse shaping, and digital-to-analog converter, has a large pile-up probability and dead time, and complicated connection [7, 5]. With growing demands for high performance, low cost and small size of DMCA systems in nuclear data acquisition, the digital signal processing (DSP) is a new approach in designing of a radiation spectroscopy system. Recently, many advanced techniques of digital pulse processing to improve DMCA have been reported in [2, 3, 4, 5, 6, 7, 8, 9]. A real-time digital trapezoidal pulse shaping was employed to increase throughput and maintain the energy resolution [6]. However, the throughput is still restricted at a high input count rate and a hardware used is expensive. A cost-effective and high performance digital signal system based on microcontroller for performing an advanced pulse processing algorithm was introduced but the input count rate is still under 61 kcps [7]. A complicated pulse shaping filter named Mexican Hat Wavelet configured on FPGA was proposed for improvement of the energy resolution and the peak-Compton ratio [8]. However, consumption of FPGA logic resources and quality of spectrum at low energy regions are still debatable to apply in low cost and high quality measurement systems.

Aiming at high performance and low cost, the DMCA was designed and implemented based on low cost FPGA. The combination of finite impulse response (FIR) and digital trapezoidal filter for shaping filter, peaks detection, pile-up rejection, baseline restoration, and spectral histogram processing are simulated and optimized by using Matlab to obtain energy resolution and minimize FPGA logic resources. Two main IC, i.e. XC7A35T (Xilinx FPGA Artix7) and AD6645 are chosen for DMCA hardware. The DMCA was tested with a HPGe detector GC1518 model of Canberra and using ^{137}Cs, ^{60}Co and ^{133}Ba standard sources.

II. PULSE PROCESSING SYSTEM DESIGN

A complex algorithm can configure a fast and large resource FPGA to obtain high performance of the DMCA but the cost is high, especially for multi-DMCA systems [8, 5, 6]. To reduce the cost of system, this work adopts two main used IC, i.e. Artix-7 XC7A35T and AD6645. The AD6645 has 14-bit resolution, and a 105 Msps sample rate. The Artix-7 FPGA family provides low power consumption, high DSP, and logic throughput in a cost-optimized FPGA [13]. To be a simple circuit, only a clock rate of 50 MHz is exploited to synchronize the clock of ADC and FPGA. The block diagram of DMCA configured on FPGA is shown in Figure 1. To enhance signal to noise ratio (SNR), a mixer using op-amp (AD847) is inserted between preamplifier and ADC to transform unipolar signal to bipolar signal.

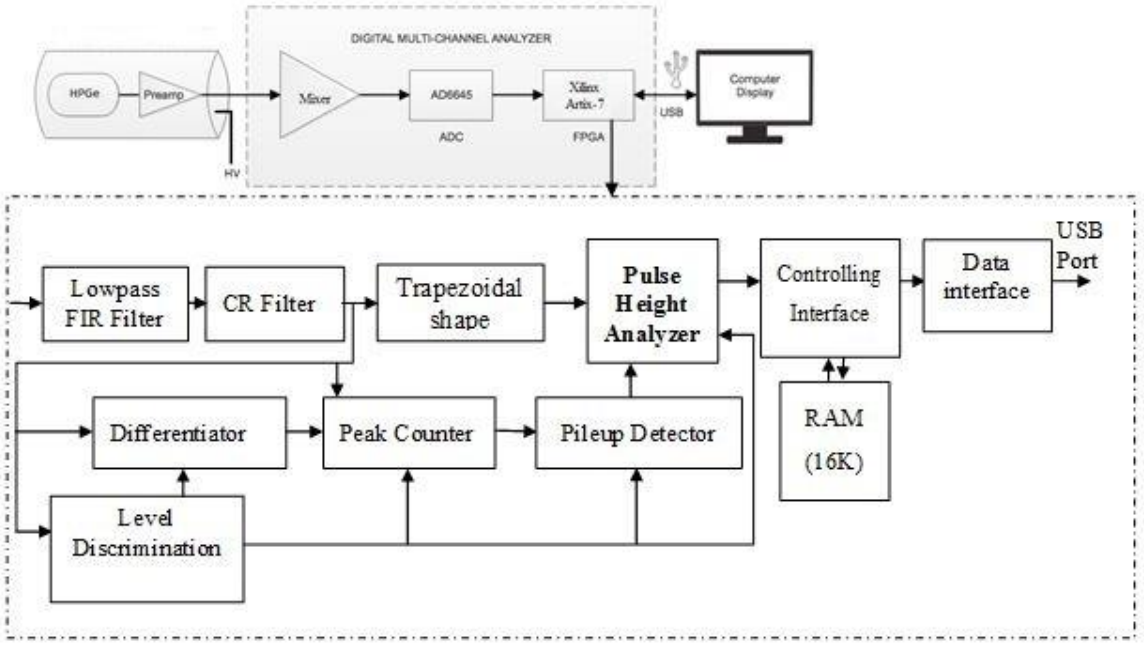

Fig.1. Schematic system of the DMCA.

The incoming signal from the preamplifier is constantly digitized by ADC and then the code of ADC is conveyed to FPGA. The pulse shaping filter, detecting peaks, spectrum histogram processing, controlling interface, and communication with computer (PC) are performed by FPGA.

The analysis algorithms such as pulse shaping filter, threshold discrimination, pileup treatment and pulse height analyzer of DMCA using raw data collecting from ADC are simulated by Matlab to inspect the performance of DMCA. A 40^{th}-order FIR low pass filter using Hamming Window with a cutoff frequency of 1.5 Mhz as Ref. [10, 11] is employed to remove high-frequency harmonics of input signal from ADC. To increase the SNR, minimize the baseline drifts and reduce pileup, the CR filter approach is next processing to filter and shorten pulse [12]. After the pulse filter, the signal moves to a signal threshold discrimination to create logic pulse for controlling next function blocks such as differentiator, peak counter, pileup detector and pulse height analyzer. The differentiator is used to reveal peaks and detect pileup. While the signal is larger than a given threshold, the peak counter counts the number peak in one pulse by using a logic pulse from a differentiator. The pileup is detected, if the number peak in one pulse is larger than one. To analyze accurately pulse height, a digital trapezoidal shaping filter is employed. Then the pulse height analyzer block detects peak of pulse and estimates baseline to calculate pulse height precisely. The code of peak is recorded in a 16384-word memory;the interface allows the PC independently to access data in memory through a USB port to display spectrum on PC.

III. RESULT AND DISCUSSION

Several benchmark tests with an HPGe detector GC1518 model of Canberra, and gamma-ray calibration sources were carried out. The experiment setup configuration is presented in Figure 2. The HPGe detector is applied at a high voltage of 2,5KV. The signal from the preamplifier output is applied directly to the DMCA and the DMCA is connected to the PC by USB cable. The DMCA uses a power supply of 5V and it has a low power consumption of 0,3W. The PC software is developed by using MATLAB to record data and display spectrum.

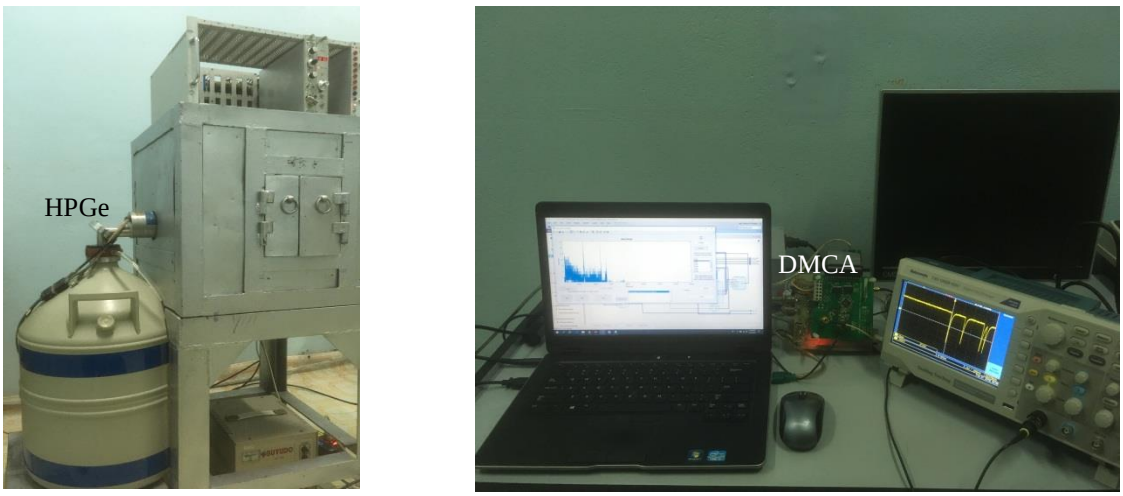

Fig.2. The experiment setup using HPGe detector of GC1518 model of Canberra.

In fig. 3 shows the gamma spectra of ^{133}Ba radioisotope source collected by the DMCA. The low energy peaks of ^{133}Ba are completely separate.

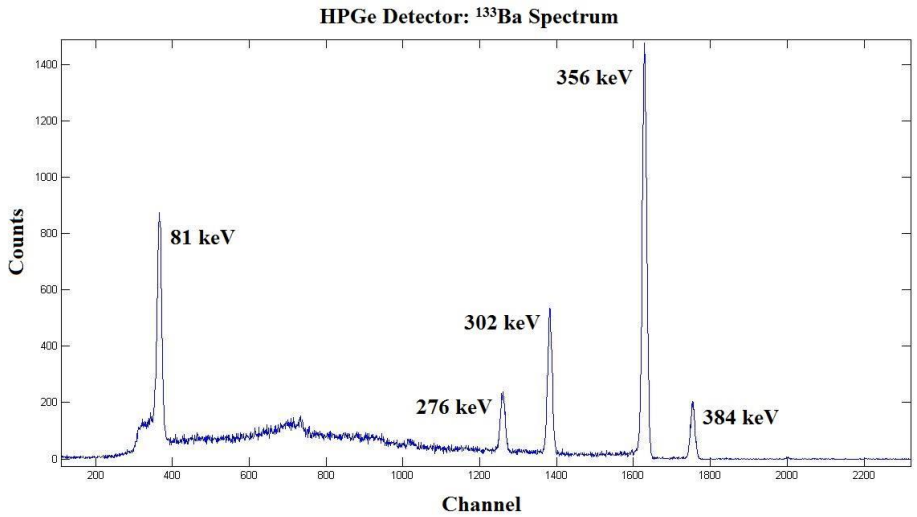

Fig. 3. The γ-ray spectrum of ^{133}Ba radioisotope source.

To examine the energy resolution of the DMCA, the peak of 1332 keV ^{60}Co is used. Fig. 4 shows the gamma spectra of ^{137}Cs and ^{60}Co radioisotope sources, the energy resolution of the DMCA at 1332 keV ^{60}Co is 3.1 keV.

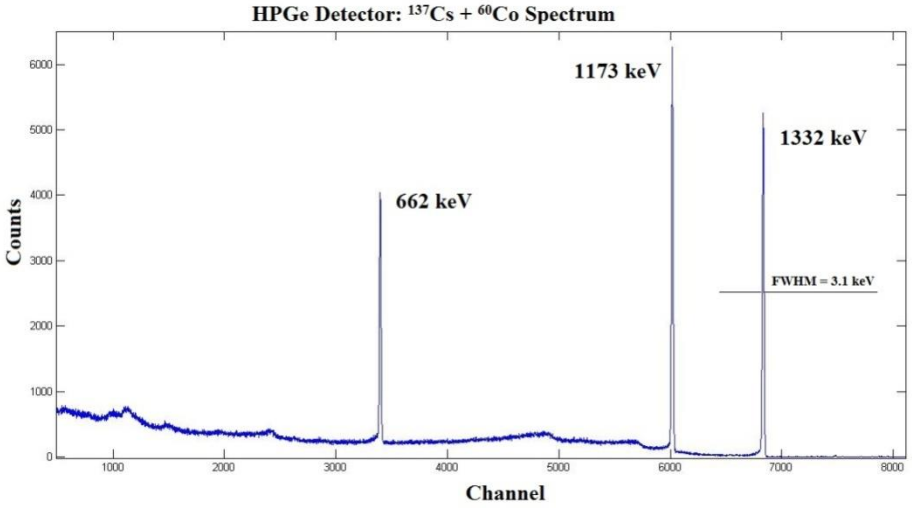

Fig.4. The γ-ray spectrum of ^{137}Cs and ^{60}Co radioisotope sources.

IV. CONCLUSION

This study reports a low-cost high-performance DMCA. The DMCA has a simple hardware, two main used IC, i.e. Artix-7 XC7A35T and AD6645. All pulse analysis algorithms are configured on FPGA. Hence, the DMCA performs in real time. The experiment results of throughput, energy resolution and quality of spectrum have shown that the performance of the proposed DMCA is remarkable.

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THIẾT KẾ HỆ PHÂN TÍNH ĐA KÊNH KỸ THUẬT SỐ DÙNG FPGA CHO ĐẦU DÒ BÁN DẪN

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Tóm tắt: Nghiên cứu này trình bày thiết kế hệ phân tích biên độ đa kênh kỹ thuật số (DMCA) dùng mạch tích hợp mảng các phần tử logic lập trình được (FPGA) cho đầu dò bán dẫn. Phần cứng chính của hệ DMCA bao gồm một vi mạch tích hợp (IC) biến đổi tương tự sang số 16 bit (ADC) với tốc độ lấy mẫu 105 Mcps và FPGA Artix-7. Các thuật toán lọc hình thành xung, xác định đỉnh và hình thành phổ kỹ thuật số được thiết kế và mô phỏng trên phần mềm MATLAB. Các tài nguyên sử dụng của FPGA được tối ưu hóa trong quá trình thiết kế và mô phỏng, dẫn đến giảm chi phí cho phần cứng của DMCA. Tất cả các chức năng được cấu hình cứng trên FPGA, nên DMCA thực thi trong thời gian thực. Chồng chập xung và ổn định đường cơ bản (baseline) được xử lý để nâng cao độ phân giải năng lượng. Hệ DMCA đã được đo thử nghiệm với đầu dò bán dẫn của hãng Canberra (model: GC1518) dùng các nguồn chuẩn ^{137}Cs, ^{60}Co và ^{133}Ba. Độ phân giải năng lượng của hệ DMCA tại đỉnh 1332 keV của ^{60}Co đạt được 3,1 keV. Kết quả bước đầu cho thấy hệ DMCA có kích thước nhỏ, chi phí thấp và hoạt động ổn định, đáp ứng tốt cho mục đích nghiên cứu và đào tạo.

Từ khóa: *DMCA, FPGA, đầu dò bán dẫn.*